In the Claims

Please replace all prior versions, and listings, of claims in the application with the following list of claims:

1. (Original) A method of transferring a multi-word data stream between a first electronic component region and a second electronic component region, said multi-word data stream having a start and a continuation, said component regions being clocked such as to have a frequency ratio therebetween variable about an average value, and a maximum mutual jitter between the two clocks the method comprising:

outputting said start from said first component region,

outputting a synchronization signal to indicate timing of outputting of said start,

outputting said continuation from said first electronic component region at a first predetermined rate,

buffering said data stream including said start and said continuation,

using said synchronization signal to establish an initial synchronization with said second electronic component region,

outputting said buffered start of said data stream to said second electronic component region in accordance with said initial synchronization, and

outputting said continuation to said second electronic component region at substantially said first predetermined rate, at timings dictated by said initial synchronization.

2. (Original) The method of claim 1, wherein said outputting of said synchronization signal is substantially together with said outputting of said start.

3. (Original) The method of claim 1, wherein said outputting of said synchronization signal is delayed by a predetermined number of clock cycles following outputting of said start, said predetermined number being selected to allow at least partial filling of said buffer.

4. (Original) The method of claim 1, wherein said component regions are both clocked using signals derived from a single clock on a third electronic component region.

5. (Original) The method of claim 1, further comprising inserting blank data within said continuation to extend said continuation and retain validity of said initial synchronization.

6. (Original) The method of claim 5, comprising adding control flags to said data stream to indicate at least one of said blank data and valid data.

7. (Original) The method of claim 1, comprising deriving said synchronization signal from a clock signal of said first region.

8. (Original) The method of claim 7, wherein said using said synchronization signal to establish an initial synchronization comprises transferring said synchronization signal to said second region, waiting for a next rising or falling edge of a second region clock signal and issuing a synchronization acknowledge signal.

9. (Original) The method of claim 1, comprising waiting after said initial synchronization before said outputting of said buffered start, thereby to establish buffering margins to cover variations in synchronization between said first and said second regions.

10. (Original) The method of claim 9, wherein said buffering margins have a minimum length of said predetermined rate multiplied by a said maximum mutual jitter.

11. (Original) The method of claim 9, wherein said buffering margins are substantially equal in size to said predetermined rate multiplied by a said maximum mutual jitter.

12. (Original) The method of claim 1, wherein said first and said second electronic component regions are regions of a single integrated circuit.

13. (Original) The method of claim 1, wherein said first and said second electronic component regions are separate integrated circuits clocked from a common originating clock signal.

14. (Original) An arrangement comprising at least one integrated circuit, said arrangement being clocked by at least one signal obtained from a single clock having variable delays to different regions of said arrangement such that said regions are partially synchronized to each other, having a mutual clock frequency ratio therebetween which varies about an average value and a maximum mutual clock jitter, the arrangement comprising:

a data transfer buffer for buffering parts of multi-word data streams during transfer between respective first and second ones of said regions, and

data transfer control functionality, associated with said data transfer buffer and said respective regions, configured to control transfer of said data stream, said functionality comprising:

synchronizing logic for detecting at least a start of transfer of said multi-word data stream, issuing a synchronizing signal based on timing at said first region, and using said synchronizing signal to form an initial synchronization with said second region, and

rate control logic for receiving data of said multi-word data stream, in said buffer, from said first region, at a predetermined rate,

said data transfer control functionality being operable to withhold forwarding of said data stream from said buffer to said second region by at least a synchronizing delay indicated by said initial synchronization, said rate control logic further being configured to carry out said forwarding to said second region at substantially said predetermined rate.

15. (Original) The arrangement of claim 14, wherein said first region comprises synchronization retention functionality to support insertion of blank data into said data stream to extend said data stream, thereby to retain validity of said initial synchronization.

16. (Original) The arrangement of claim 15, wherein said synchronization retention functionality comprises functionality to insert control flags into said data stream to indicate at least one of said blank data and valid data.

17. (Original) The arrangement of claim 14, wherein said initial synchronization comprises sending said synchronization signal from said first region to said second region simultaneously with outputting of a start of said data stream from said first region.

18. (Original) The arrangement of claim 14, wherein said data transfer buffer comprises a FIFO stack.

19. (Original) The arrangement of claim 14, wherein said first and said second regions are located on a single integrated circuit.

20. (Original) The arrangement of claim 19, wherein said single integrated circuit comprises very large scale integration (VLSI).

21. (Original) The arrangement of claim 14, wherein said synchronization signal is a derivation of a first region clock signal.

22. (Original) The arrangement of claim 21, wherein said synchronizing logic comprises logic associated with said second region for producing a synchronize acknowledgement at a first rising or falling edge of a second region clock signal following receipt of said synchronizing signal.

23. (Original) The arrangement of claim 22, wherein said buffer is configured to introduce a forwarding delay following receipt of said synchronize acknowledgement before forwarding said data stream to said second region.

24. (Original) The arrangement of claim 23, wherein said buffer comprises a plurality of buffer units to buffer variable amounts of data, said forwarding delay being selected to leave margins within said buffer both for transient increasing and decreasing of a buffer storage level, thereby to cushion transient changes due to a mutual clock jitter relationship between said regions.

25. (Original) The arrangement of claim 24, wherein said forwarding delay is selected such as to render said margins substantially equal in size.

26. (Original) The arrangement of claim 24, wherein said forwarding delay and a number of said buffer units are selected such as to provide a margin size at least equal to said predetermined rate multiplied by a maximum of said mutual clock jitter.

27. (Original) The arrangement of claim 24, wherein said forwarding delay and a number of said buffer units are selected such as to provide a margin size substantially equal to said predetermined rate multiplied by a maximum of said mutual clock jitter.

28. (Currently amended) A method for transferring a stream of data between a first electronic component region and a second electronic component region the operation of which is phase-independent of the first electronic component region, said regions clocked from a commonly originating clock signal such that a clock frequency ratio variable about an average value is established between said regions, the method comprising:

buffering said data stream received from said first region at a predetermined rate,

initially synchronizing receipt of buffering output at the second region with phasing of a clock of said second region in response to a synchronization signal from the first region, and

outputting said buffered data to said second region continually at said predetermined rate according to said initial synchronization.